APPENDIX

Claims 1, 2, 9, 13 and 15 now read as follows.

1. (Amended) A semiconductor device, comprising:

conductive transfer gates;

contact plugs adjacent to said conductive transfer gates, each contact plug and each conductive transfer gate having a respective upper surface, wherein the upper surfaces of the contact plugs and the upper surfaces of the conductive transfer gates are substantially coplanar;

said each conductive transfer gate having a gate insulating film,

a gate electrode layer, and side walls for covering sides of said gate insulating film and said gate electrode layer;

a first interlayer insulating film having a surface which defines the same surface as the upper surfaces of said conductive transfer gates and said contact plugs;

a second interlayer insulating film formed on said first interlayer insulating film; and

diameter-reduced contact plugs which are smaller than said contact plugs and extend through said second interlayer insulating film to conduct to said contact plugs, respectively.

2. (Twice Amended) The semiconductor device according to claim 1, further including a memory cell section having a plurality of memory cells,

said memory cell section including, in addition to said conductive transfer gates, said contact plugs, and said first and second interlayer insulating films,

a bit line formed on said second interlayer insulating film;

a third interlayer insulating film formed on said second interlayer insulating film so as to cover said bit line; and

capacitors formed on said third interlayer insulating film;

said memory cell section further including said diameter-reduced contact plugs, which include

a bit line contact plug which extends through said second interlayer insulating film to bring said contact plugs and said bit line into conduction; and

a capacitor contact plugs which extend through said second and third interlayer insulating films to bring said contact plugs and said capacitors into conduction.

9. (Twice Amended) The semiconductor device according to claim 1, further including a logic circuit section including a plurality of transistors, said logic section including, in addition to said conductive transfer gates, said contact plugs, and said first and second interlayer insulating films,

bit lines formed on said second interlayer insulating film; and

said logic circuit section further including, as said diameter-reduced contact plugs,

bit line contact plugs which extend through said second interlayer insulating film to bring said contact plugs and said bit lines into conduction.

13. (Amended) The semiconductor device according to claim 1, wherein the gate electrode layer of said conductive transfer gate has a metal layer and a barrier metal which surrounds the metal layer.

15. (Amended) The semiconductor device according to claim 1, wherein the gate insulating film of said conductive transfer gate is a thermal oxide film formed by a thermal

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oxidation method or a thermally-oxidized nitride film formed by a thermal oxidation nitriding method.